



Indira Gandhi Delhi Technical University For Women
(Established by Govt. of Delhi vide Act 09 of 2012)
Kashmere Gate, Delhi-110006
Department of Electronics & Communication Engineering
TIME TABLE

F-AD-03

Even Sem Jan-May 2022/ B. Tech 2nd Semester M Tech (VLSI)

w.e.f: 12th Jan 2022

Time	9-10 AM	10-11 AM	11-12 AM	12-1 PM	1-2 PM	2-3 PM	3-4 PM	4-5 PM
Day								
Mon	RM		DMCS	ANNDL		DVD	DVD lab	
Tue	RM		DMCS	ANNDL		DVD	AEV	AEV(T)
Wed	RM		DMCS	ANNDL		DVD	LPVD	
Thu			DMCS (T)	AEV		LPVD	LPVD Lab	
Fri		ANNDL lab		AEV		LPVD		

Sub. Code	Lab/ Course Name	Faculty Name
MVD-102	Digital VLSI Design: DVD (Th+Lab)	Dr S S Rajpoot : Contact 9871655903
MVD-104	Advances in Emerging VLSI: (Th+ Tutorial)	Prof Jasdeep Kaur
MVD- 132	Artificial Neural networks & Deep Learning: (Th+lab)	Prof Nidhi Goel
MVD-120	Low Power VLSI Design: (Th+lab)	Prof Vandana Niranjana
MVD-106	Device Modelling and Circuit Simulation: (Th+Tutorial)	Mr Wazir Singh: Contact 9896522697
ROC-101	Research Methodology & Publication Ethics (RM)	Ms Monika from CSE

Prof Nidhi Goel

(HOD, ECE)

Ms Greeshma Arya

(Time Table In-charge, ECE Dept)



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Prof Nidhi Goel

(HOD, ECE)

A handwritten signature in red ink, appearing to read 'Greeshma Arya', is positioned above the printed name.

Ms Greeshma Arya

(Time Table In-charge, ECE Dept)